

JC720 U.S. PTO
10/035078

12/28/01

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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10035078	12/28/2001	257	673	2826	Williams

****APPLICANTS:** Grigg Ford; Farnworth Warren;

****CONTINUING DATA VERIFIED:**

THIS APPLICATION IS A CON OF 09/569,216 05/11/2000 PAT 6,337,511
WHICH IS A DIV OF 09/176,967 10/22/1998 PAT 5,248,611
WHICH IS A CON OF 08/916,977 08/14/1997 PAT 5,840,598

**** FOREIGN APPLICATIONS VERIFIED:**

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		3134.7US (96-1171.7)
Verified and Acknowledged Examiners's initials		
TITLE : LOC Semiconductor assembled with room temprature adhesive		

U.S. DEPT. OF COMM. / PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg. Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		Application Examiner	
		PREPARED FOR ISSUE	
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